REMARKS

Reconsideration of the above referenced application in view of the following

remarks is requested. Paragraph [0003] of the specification has been amended to

correct a couple of editorial errors. Existing claims 1-33 remain in the application.

ARGUMENT

Information Disclosure Statement

The information referred to by the foreign patent document (WO 00/52582) in the

information disclosure statement filed on 9/12/03 has not been considered for failure to

comply with 37 CFR 1.98(a)(3).

The WO 00/52582 reference is a publication in German of a PCT application filed

on September 08, 2000. The U.S. is a designated country. Applicants are searching

whether the application has entered the national phase in the U.S. and/or whether it has

a corresponding English publication. An updated information disclosure statement will

be filed upon the search results.

Claim Rejections – 35 USC § 112

Claims 11, 14, 18, 21, 24, and 28 are rejected under 35 U.S.C. § 112, first

paragraph, as failing to comply with the enablement requirement.

The Examiner rejected these independent method claims for the reason that the

phrase "inner relationship" was not described in the specification as to enable one of

ordinary skill in the art to make and/or use the invention. Applicants hereby respectfully

disagree with this assertion by the Examiner. There is no requirement that claims use

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the exact terms used in the specification. Throughout the specification, Applicants use

words "inner" and "outer" to describe L1 caches and L2 caches, respectfully, shown in

Figure 1 which is a base figure for all other figures in the application (e.g., see

paragraph [0014] of the specification). The phrase "inner relationship" can be inferred

from the specification and be readily understood by one person of ordinary skill in the

art. Therefore, Applicants respectfully request that the 35 U.S.C. § 112 rejection over

claims 11, 14, 18, 21, 24, and 28 be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Claims 1 and 31 are rejected under 35 U.S.C. § 102(e) as being anticipated by

Arimilli et al. (US 6,629,268) (hereinafter Arimilli 1).

A claim is anticipated under §102 "only if each and every element set forth in the

claim is described, either expressly or inherently, in a single prior art reference." See

MPEP § 2131 (Quoting Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628,

631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). Applicants submit that the Examiner has

failed to establish a prima facie case of anticipation because Arimilli\_1 fails to teach a

cache accessible from said first interface and said second interface, to contain a cache

line with a first cache coherency state when accessed from said first interface and a

second cache coherency state when accessed from said second interface, as recited in

claims 1 and 31.

The Examiner made the above rejections by relying on Fig. 2 and col. 8, lines 6-

33 of Arimilli 1. Fig. 2 does not show any cache line of L2 cache (12) with a cache

coherency state. Col. 8, lines 6-33 does not disclose **TWO** cache coherency states, i.e.,

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a first cache coherency state when accessed from said first interface and a second

cache coherency state when accessed from said second interface. The only place of

col. 8, lines 6-33 that mentions something related to a cache coherency state is in line

30: "updates a coherency state indicator ...." This phrase in col. 8, line 30 of Arimilli\_1

has nothing to do with TWO cache coherency states. Thus, the cited portions of

Arimilli 1 do not teach or suggest a cache line with a first cache coherency state when

accessed from said first interface and a second cache coherency state when accessed

from said second interface. Applicants hereby respectfully request that the 35 U.S.C. §

102 rejections over claims 1 and 31 be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 2-10 and 32-33 are rejected under 35 U.S.C. §103(a) as being

unpatentable over Arimilli 1 in view of Arimilli (US 2002/0129211) (hereinafter

Arimilli\_2).

For reasons presented above in traversing the 35 U.S.C. § 102 rejections over

claims 1 and 31, these two independent claims are allowable over Arimilli\_1. A review

reveals that Arimilli 2 does not teach or suggest TWO cache coherency states

associated with a cache line. Claims 2-10 depends from independent claim 1 and

claims 32-33 depends upon independent claim 31. Hence, the combination of Arimilli 1

and Arimilli\_2 does not teach or suggest at least the element of TWO cache coherency

states associated with a cache line. Therefore, claims 2-10 and 32-33 are allowable

over Arimilli 1 in view of Arimilli 2. Applicants hereby respectfully request that the 35

U.S.C. § 103 rejections over these dependent claims be withdrawn.

Claims 11-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over

Arimilli\_2 in view of Arimilli (US 6,341,336) (hereinafter Arimilli\_3).

Regarding claim 11, the Examiner asserted that Arimilli 2 discloses associating a

first cache coherency state with a first cache line in a first cache (paragraph [0010]) and

associating a second cache coherency state with a second cache line in a second

cache in an inner relationship to said first cache (paragraphs [0024] and [0029]); and

Arimilli 3 discloses (or renders obvious) transitioning a first cache coherency state to a

joint cache coherency state including said first cache coherency state for outer

interfaces and a third cache coherency state for inner interfaces (col. 4, line 60 to col. 5,

line 15) and transitioning said second cache coherency state to said third cache

coherency state (col.5, line 47 to col.6, line 4; col. 5, lines 16-34). This assertion is

incorrect as to each element recited in claim 11. To be succinct, Applicants here points

out only one of several mistakes the Examiner made in the above assertion.

The cited portion of Arimilli 3 (col.4, line 60 to col. 5, line 15) does not teach or

suggest the element of transitioning a first cache coherency state to a joint cache

coherency state including said first cache coherency state for outer interfaces and a

third cache coherency state for inner interfaces. The cited portion of Arimilli 3 discloses

an intervention procedure regarding a cache line having a Modified state for the

purpose of reducing write-back (to system memory) operations. The cited portion

specifically discloses how the cache coherency state of the cache line changes

during/after the procedure: "At the end of the procedure, the cache which held the data

in the Modified state will switch to the Shared state, and the other processor's cache

Application No.: 10/662,093 Filed: 09/12/2003 block will go from the Invalid state to the Shared state as well ..." (col.4, line 64 to col.5,

line 1 of Arimilli 3). To avoid unnecessary writes to system memory, Arimilli\_3

discloses a method of maintaining cache coherency in a multi-processor computer

system using a "Tagged" coherency state instead of Modified state for a particular

cache line (see col.5, line 47 to col.6, line 32 of Arimilli\_3). Such a Tagged coherency

state is simply a single cache coherency state line ones such as "Modified, Exclusive,

Shared, and Invalid," and is NOT a joint cache coherency state including TWO

conventional cache coherency states as recited in claim 11. Additionally, what is

disclosed in Arimilli 3 does not evidence that the joint cache coherency state element is

well known as asserted by the Examiner because a single new state (i.e., Tagged) only

a particular cache line with a conventional Modified state is totally different from a joint

cache coherency state including TWO conventional cache coherency states, which is

used for any cache line in an outer-level cache. Furthermore, a review of Arimilli\_2

does not teach or suggest the claimed joint cache coherency state element either.

Therefore, the combination of Arimilli 2 and Arimilli 3 does not teach or suggest this

element as recited in claim 11.

Because the combination of Arimilli 2 and Arimilli 3 does not teach or suggest

all of the elements recited in claim 11, this independent claim is thus allowable.

Independent claims 14, 18, 21, 24, and 28 are rejected for the same reasons

used to reject claim 11. For reasons presented above in traversing the rejections of

claim 11, these independent claims are allowable over the combination of Arimilli 2 and

Arimilli 3.

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Because independent claims 11, 14, 18, 21, 24, and 28 are allowable over Arimilli\_2 in view of Arimilli\_3, all of the claims that depend therefrom (i.e., claims 12-13, 15-17, 19-20, 22-23, 25-27, and 29-30, respectively) are also allowable over Arimilli\_2 in view of Arimilli\_3.

Therefore, Applicants respectfully request that the 35 U.S.C. § 103 rejections of claims 11-30 over Arimilli 2 in view of Arimilli 3 be withdrawn.

## CONCLUSION

In view of the foregoing, existing claims 1-33 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Early issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,

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